

Fig. 1

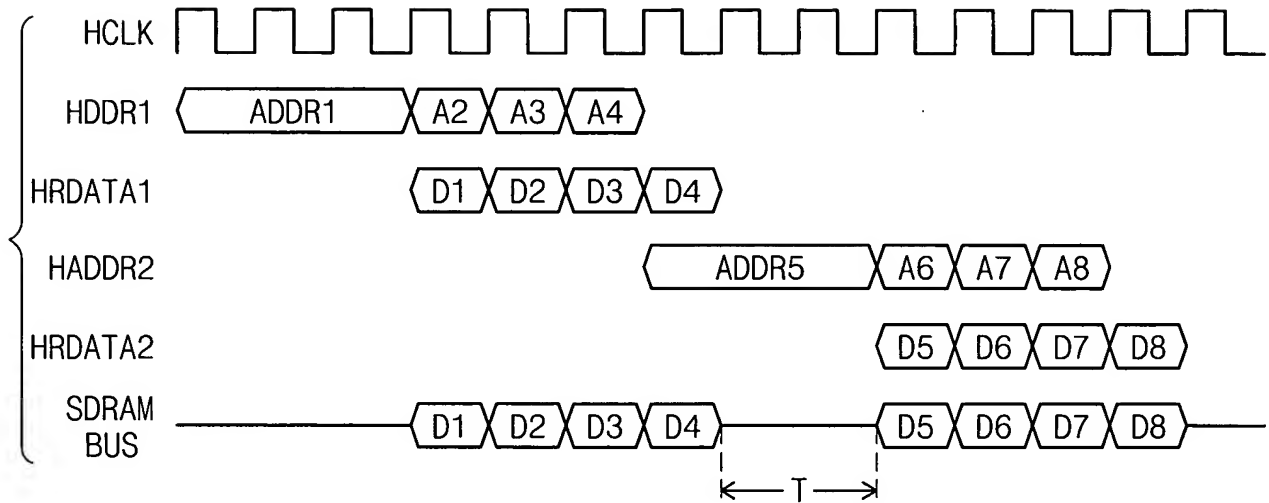


Fig. 2

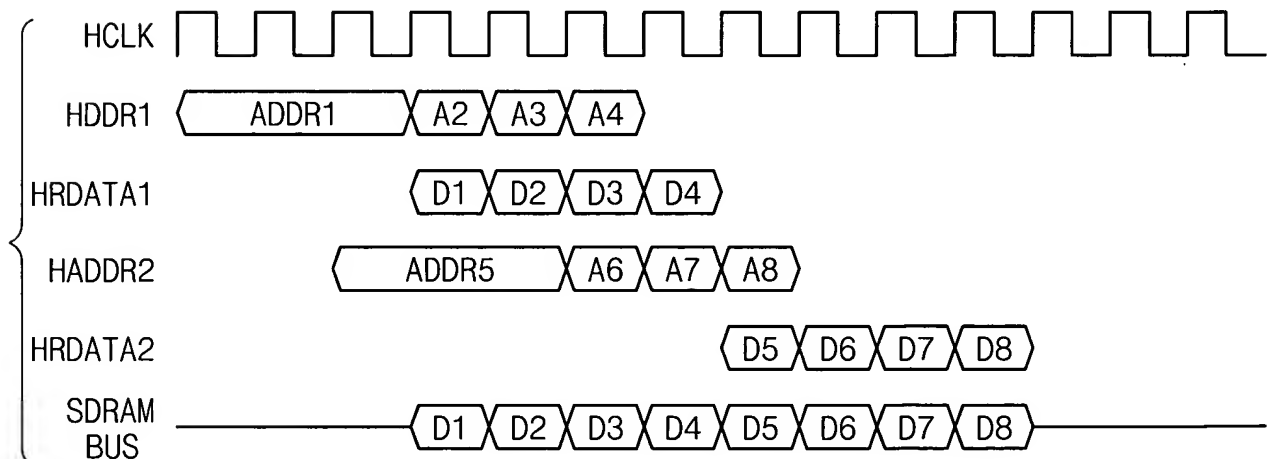


Fig. 3

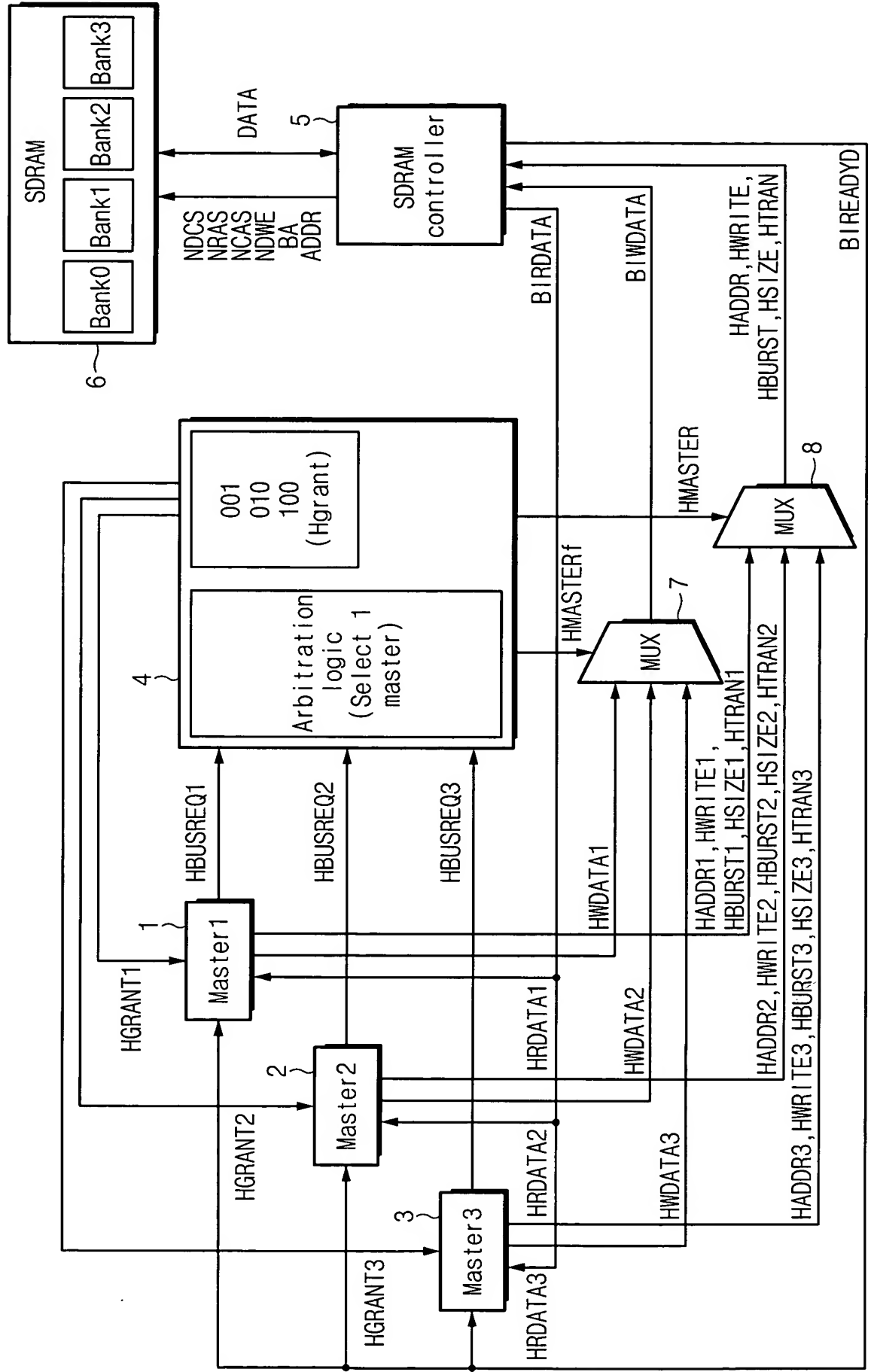


Fig. 4

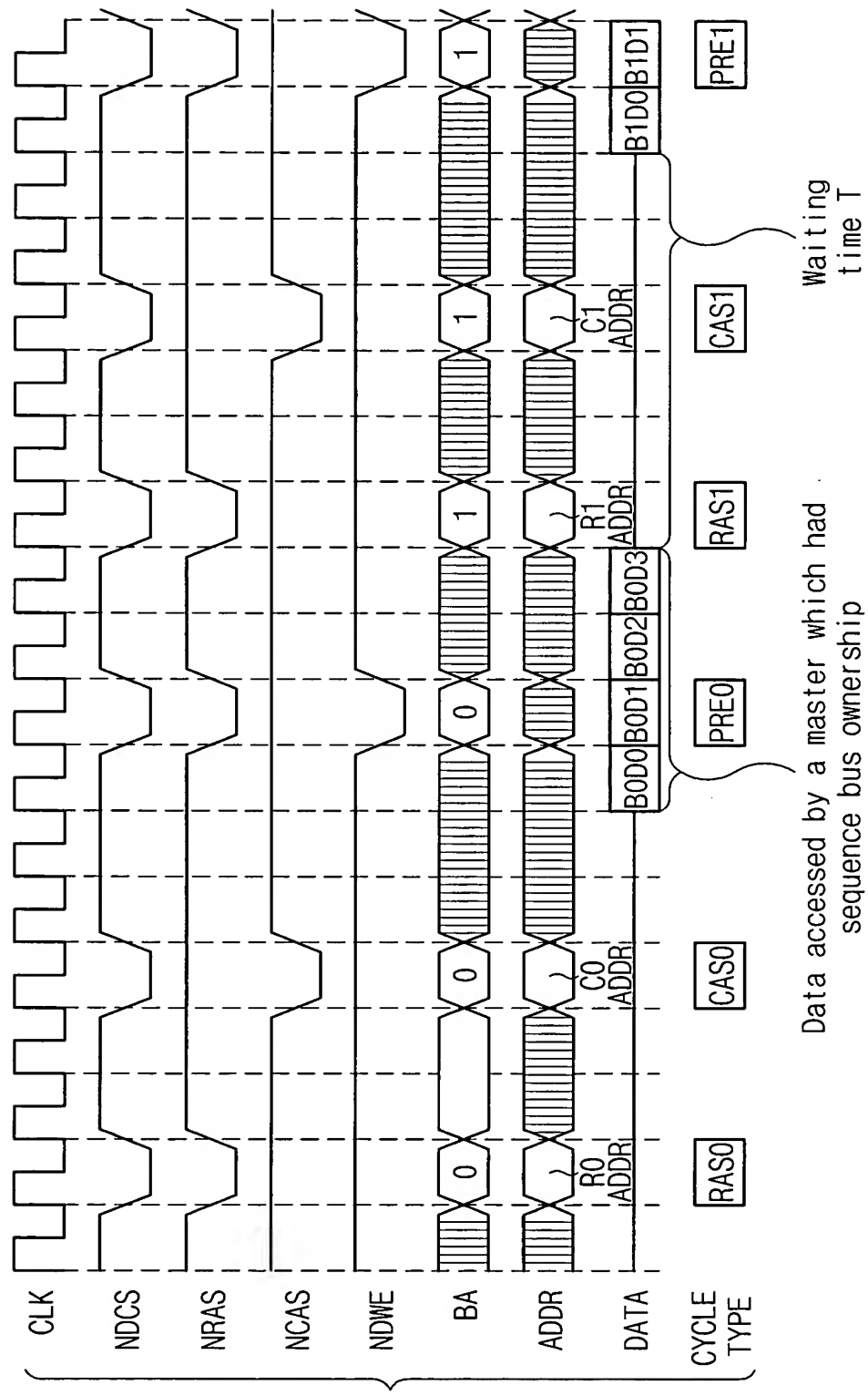


Fig. 5

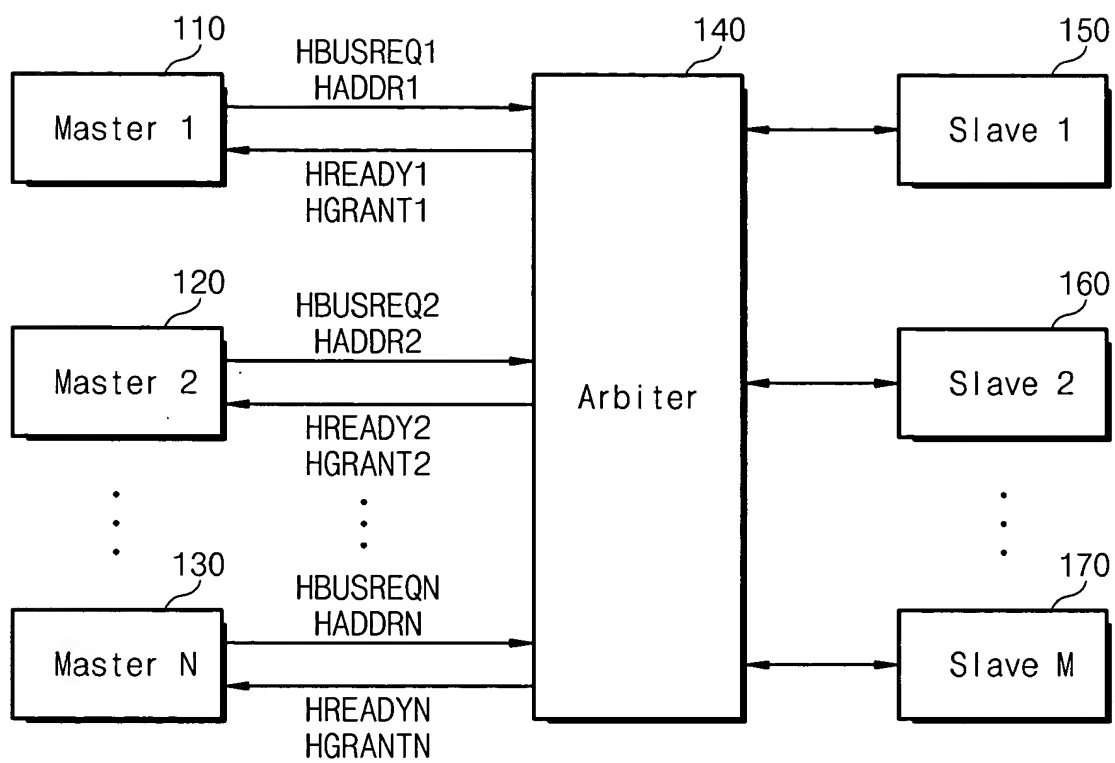


Fig. 6

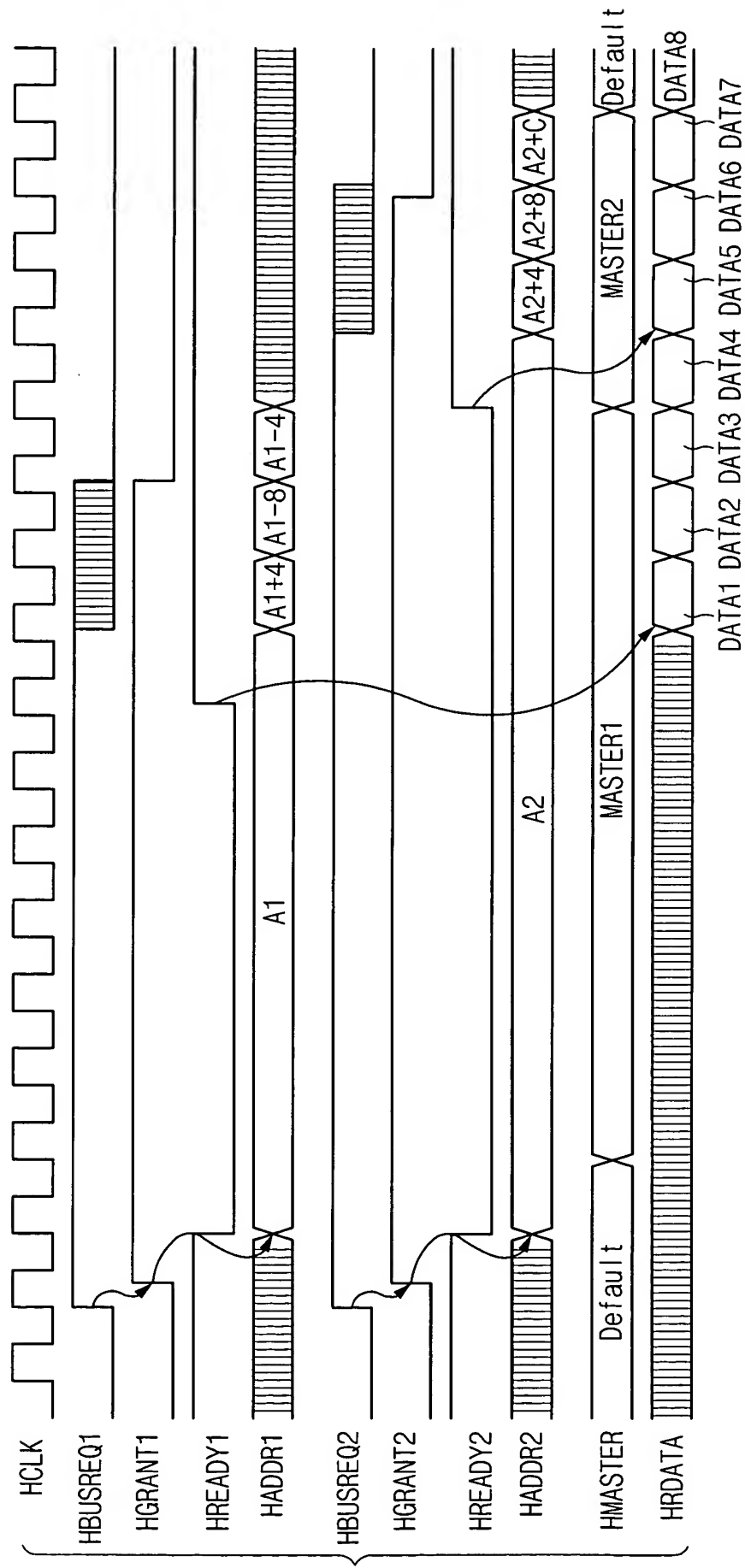


Fig. 7

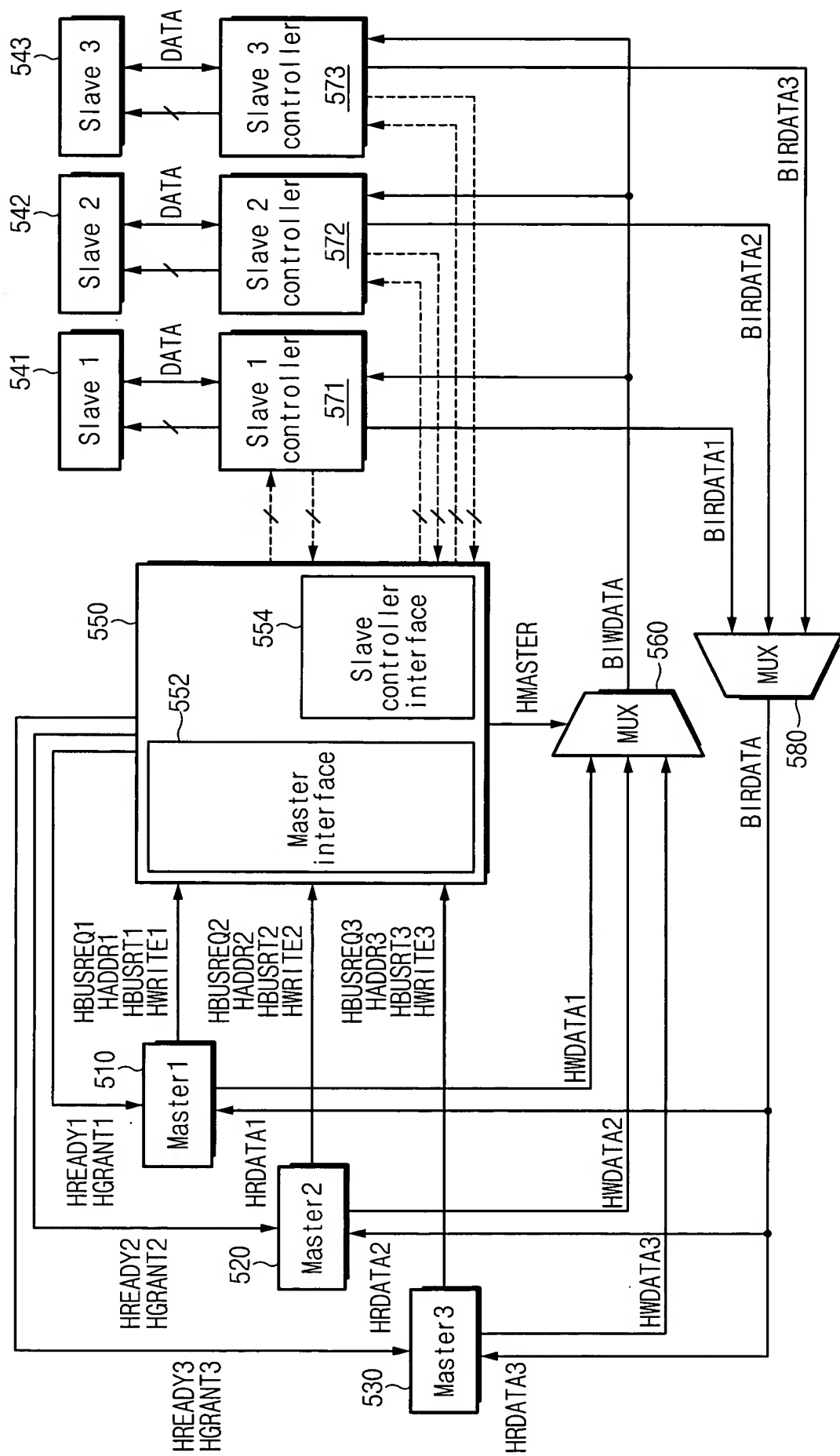


Fig. 8

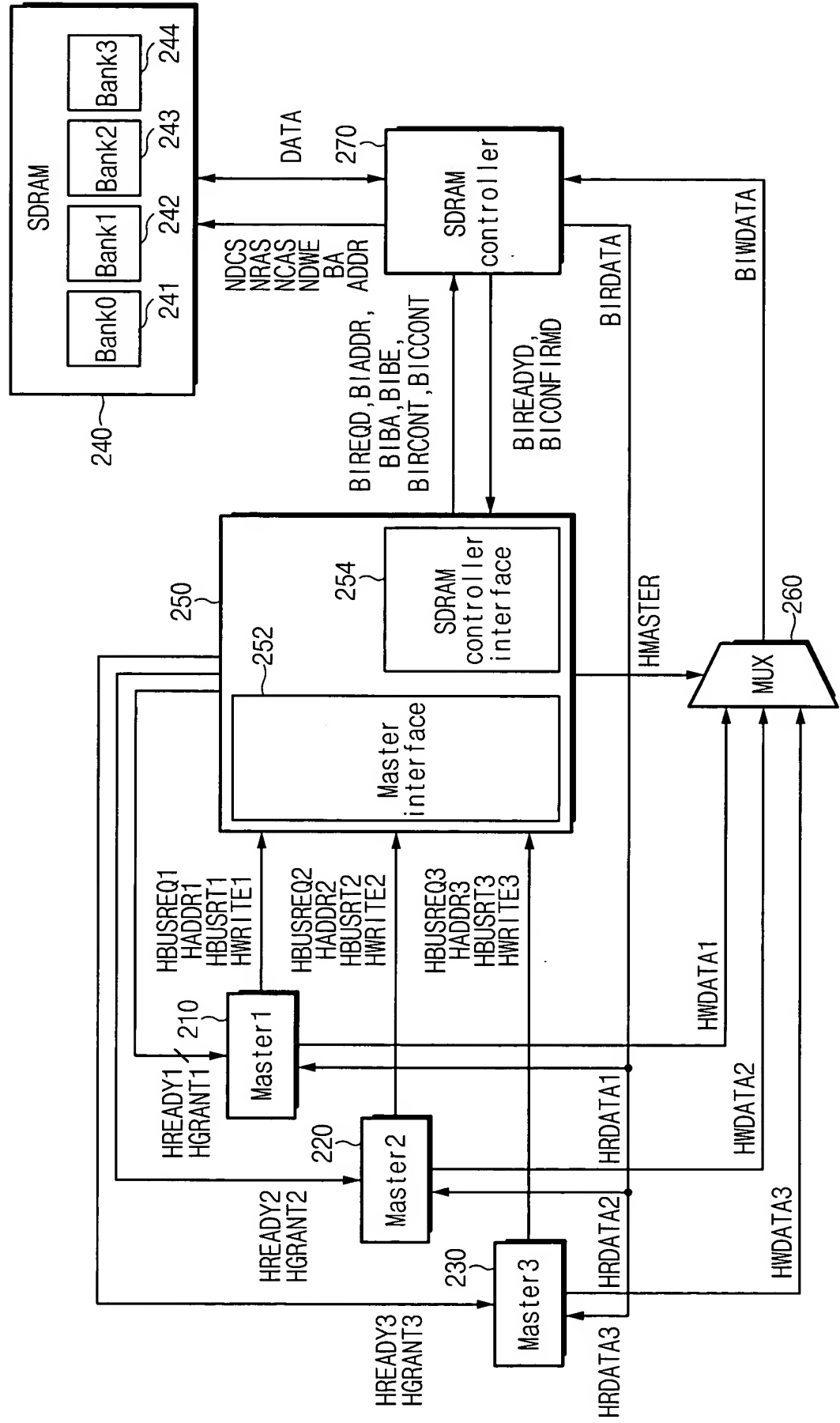
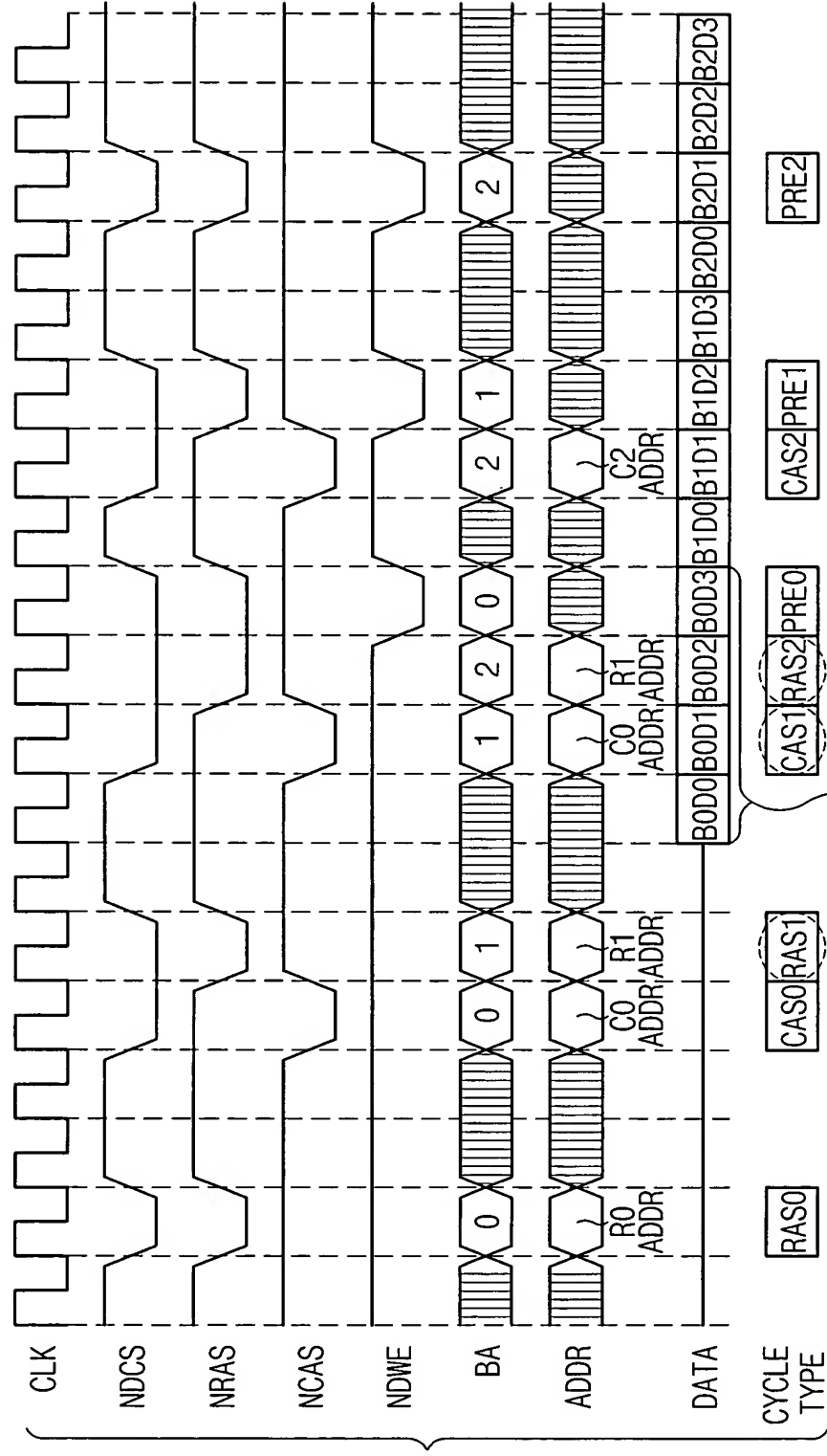


Fig. 9



Data accessed by a master which had
sequence bus ownership

Fig. 10

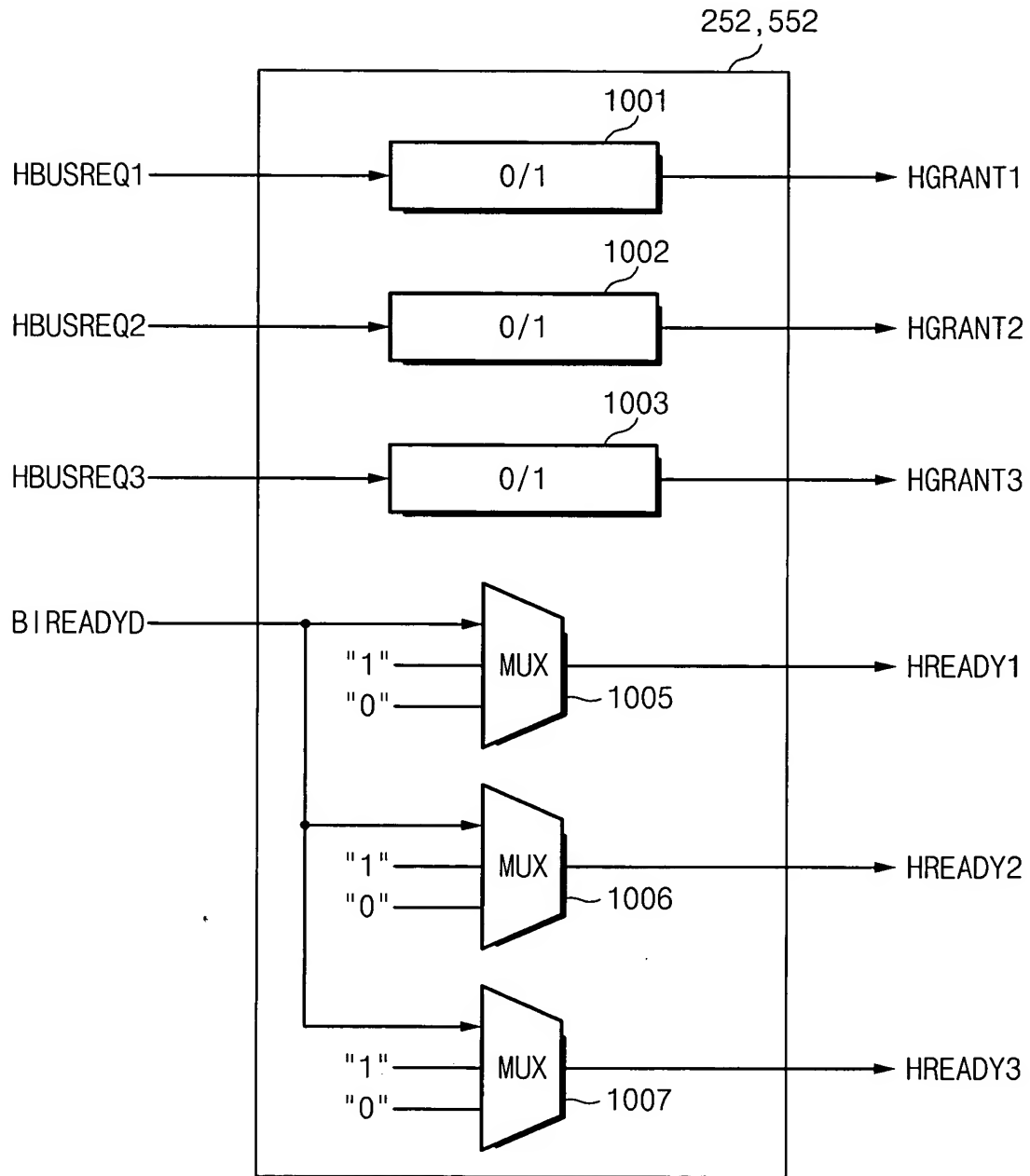


Fig. 11

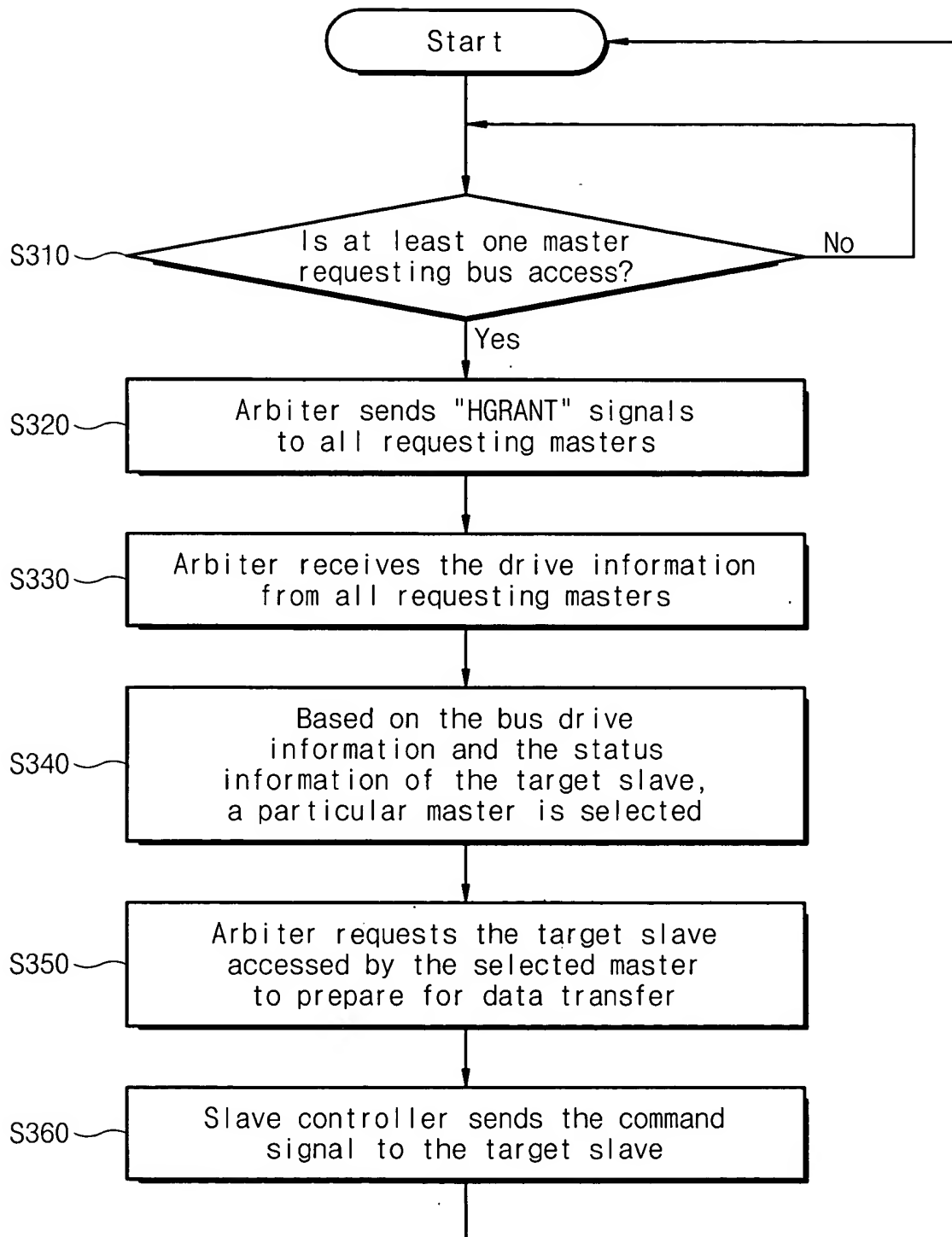


Fig. 12

